Title of Investigation:

Monocrystalline Substrates for Antenna-Coupled Sensors

Principal Investigator:

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Initiation Year:

FY 2005

Aggregate Amount of Funding Authorized in FY 2004 and Earlier Years:

$0

Funding Authorized for FY 2005:

$26,000

Actual or Expected Expenditure of FY 2005 Funding:

Contracts: $500 to Anritsu for RF connectors; $500 to custom microwave for test fixture fabrication; $1,100.00 to K.H. Sales for alignment fixture; $15,000 to MEI Corporation for labor to fabricate device development laboratory; $700 to Micro-Mark for tools; $1,200 to Northrop Grumman for masks; $2,200 to Testmart for connectors; $800 to Times Microwave for RF test cables; $1,000 to Transera Corporation for calibration software; and $2,400 to Urtrasil Corporation for silicon wafers

Status of Investigation at End of FY 2005:

Project placed on hold in FY 2005 due to funding problems

Purpose of Investigation:

Our goal in this investigation is to demonstrate a low-loss single crystal guiding structure for superconducting transmission lines between high-frequency antennas and high-performance sensors. The structure (substrate) needs to be compatible with silicon-processing techniques used in the fabrication of background-limited detectors. Although the use of single-crystal silicon for this purpose is theoretically well motivated, the suggested innovation is inherently high risk; but holds the promise to enable a new class of instrument concepts.

Superconducting-transmission lines are commonly used as circuit elements in antenna-coupled millimeter and sub-millimeter wave sensors. The attenuation in these lines can be traced to loss in the dielectric substrate, loss in the metallization, and spurious radiation from discontinuities. In practice, this is a limiting factor in the application of this approach in realizing a greater degree of system complexity, miniaturization, and resolution in a broad class of instruments. The measured loss in niobium superconducting transmission lines is currently dominated by the silicon-oxide dielectric employed. The observed dissipation is temperature independent and characterized by loss tangent of $\sim 5.4 \times 10^{-3}$ and believed to be a result of disorder in the thin-film substrate. Dielectric losses at this level will result in power attenuation of a few percent per wavelength at millimeter wavebands.

Accomplishments to Date:

We have investigated the use of single-crystal silicon as a low-loss substrate material for superconducting-microstrip transmission lines. We have designed and fabricated test structures and fixtures to enable precision-dielectric measurements. Two wafer runs, with ring resonator test structures, were fabricated and characterized at multiple harmonics up to ~40 GHz during the course of this investigation. The transmissions lines were realized by metalizing one side of an silicon insulating oxide (SIO) wafer with niobium, etching down to the insulating stop, and patterning this thin substrate surface with the desired test circuit. See Figure 1 for the substrate geometry.

To achieve the desired measurement accuracy, ring resonator structures were measured at multiple harmonics, three different line widths, and two different resonator-coupling strengths. We have developed a novel algorithm to determine the unloaded quality factor, effective dielectric constant, loss tangent, and surface resistivity of the superconductor. Further effort on the data reduction technique is ongoing. A typical ring-resonator test structure in the measurement carrier is shown in Figure 2. The test set-up and preliminary data from a few of the structures are presented in Figures 3 and 4, respectively. From the data taken at multiple couplings and harmonics, we have derived an upper bound on the loss tangent for the material of $\sim 5 \times 10^{-5}$. Further refinements in our measurement and data-analysis techniques are anticipated to improve this conservative upper bound.

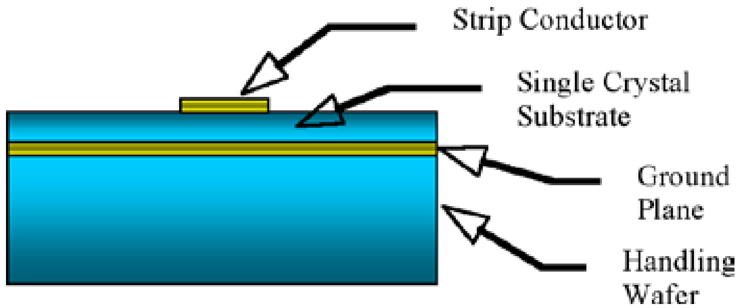

Figure 1. Superconducting-microstrip line with single crystal substrate geometry

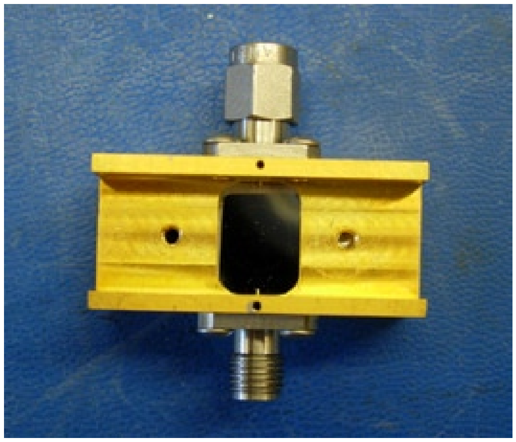

Figure 2. Monocrystalline-silicon, microstrip-ring resonator mounted in test fixture

Figure 3. HP8510C network analyzer and cryostat used for test of microstrip test structures

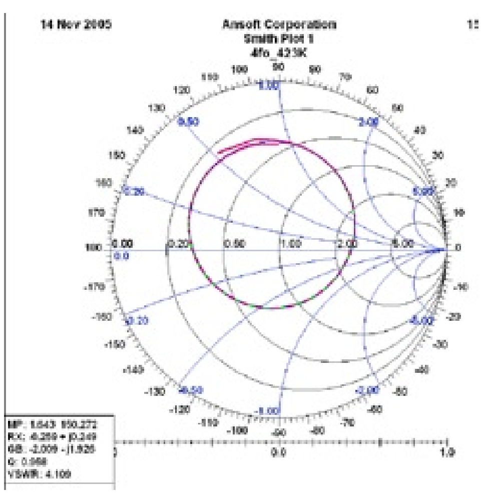

Figure 4. Scattering parameter plot of the measured (magenta lines) and curve fitted (green dashed lines) of the ring resonator at 4.22 Kelvin

Key Points Summary:

Project's innovative features: An innovative fabrication process was proposed for superconducting transmission lines with monocrystalline substrates. The approach has the potential to significantly reduce the dominant loss mechanism for this class of high-frequency interconnects.

Potential payoff to Goddard/NASA: Successful demonstration of the desired low-loss properties will enable the development of a new class of instrument architectures compatible with antenna-coupled sensors with improved sensitivity and resolution. The substrate studied shows good potential for use in the low background missions (e.g., CMBPol, SOFIA, SPECs, etc.). The capability to route high-frequency signals with low loss will enable the development of new classes of compact high-performance spectrometers for wavelengths longer than ~600 μm. Such devices would bring important new capabilities for early universe studies and enable high-performance redshift surveys.

The criteria for success: The two important milestones for this work were the ability to precisely measure dielectric properties at cryogenic temperatures and demonstrate a low-loss guiding structure appropriate for use at millimeter wavelengths. Both were achieved. A success criterion for this innovation is seeing a transmission loss that is compatible with greater-than-meter scale interconnect runs. The candidate substrate microstrip configuration was able to achieve greater than a factor of 10 reduction in dielectric loss over conventional material systems.

Technical risk factors: It was unclear if the thin substrate used for the test-chip design could be carried through fabrication and test without damage. By appropriate modification of existing fabrication processes acceptable yield was achieved. Further modification of the chip test fixture is planned in order to facilitate mounting of the device without risk of damage during test.